#8/D
7/11/02
DSS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kinji SAIJO et al
IA No.: PCT/JP00/03746
IA Filed: May 9, 2000
U.S. App. No.: 10/009,196
National Filing Date: December 10, 2001
For:

Art Unit:

Washington, D.C.

MONDAY, April 15, 2002

Docket No.: SAIJO=7

SUPPLEMENTAL AMENDMENT

Honorable Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

Prior to examination upon the merits, kindly amend as follows:

IN THE CLAIMS

Please amend claims 4 and 6 as follows:

B1 Sub C8

4. (Amended) An interposer for use in a semiconductor device in which a clad plate as defined in any one of claims 1 or 2 is etched selectively to form connecting bumps with a semiconductor chip and a wiring layer, the semiconductor chip and the wiring layer are connected by way of the semiconductor chip connection bumps using anisotropically conductive adhesives and conduction of the interposer in the direction of the thickness is taken by way of a columnar conductor formed by etching.

B2 Cont Sub C8

6. (Amended) A method of manufacturing an interposer-forming clad layer for use in a semiconductor device as defined in any